AAT2749

SystemPower™

3.0MHz Step-Down Converter and Low V_{IN} LDO

General Description

The AAT2749 is a two channel power regulator that operates from 2.3V to 5.5V. The AAT2749 contains a 3.0MHz, 600mA step-down converter and a low input voltage 300mA LDO regulator.

The step-down converter can deliver 600mA of load current. The 3.0MHz switching frequency minimizes the size of external components while keeping switching losses low. The AAT2749 step-down converter maintains high efficiency throughout the operating range, which is critical for portable applications. Fixed frequency, low noise operation can be forced by a logic signal on the MODE pin.

The AAT2749 also contains a 300mA LDO regulator with input voltage capability as low as 1.62V. The LDO regulator power input can be tied directly to the output of the step-down regulator to increase efficiency.

Total quiescent current for the step-down converter and LDO is a low 100µA under no load condition.

The AAT2749 is available in a Pb-free, space-saving 9-pin chip scale package (CSP) (200µm bump in 400µm pitch) and is rated over the -40°C to +85°C temperature range.

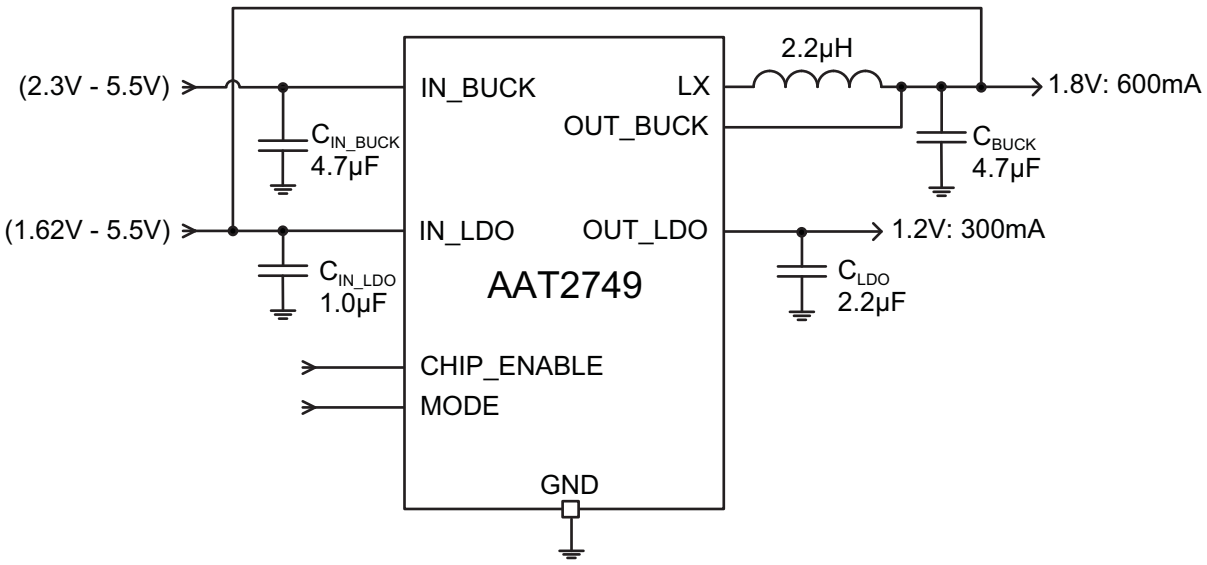
Features

- V_{IN} Range: 2.3V to 5.5V
- Two Outputs
  - V_{OUT_BUCK} = 1.8V
  - V_{OUT_LDO} = 1.0V, 1.2V
- Step-Down Converter
  - Ultra-Small 0603 Inductor (Height 1mm)
  - Up to 92% Efficiency
  - 3.0MHz Switching Frequency
  - MODE Selection Pin to Select Forced PWM or PWM/LL Operation Mode
  - Current Limit Protection
  - Automatic Soft Start
- LDO Regulator
  - V_{INL} Range: 1.62V to V_{IN}
  - 300mA Output Current
  - Current Limit Protection
- 100µA No Load Quiescent Current
- Over-Temperature Protection
- -40°C to +85°C Temperature Range

Applications

- Battery-Powered Applications
- Cellular and Smart Phones
- Digital Still and Video Cameras
- PDAs, Palmtops
- Portable Instruments

Typical Application

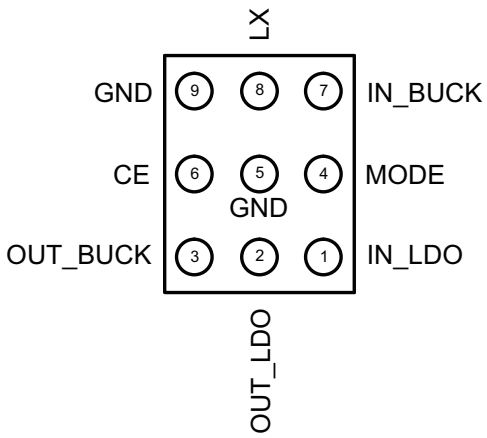


Pin Descriptions

Pin #	Symbol	Description
1	IN_LDO	Input supply voltage for the LDO regulator. May be connected to output of step-down regulator.
2	OUT_LDO	LDO power output.
3	OUT_BUCK	Step-down converter output voltage feedback pin.
4	MODE	Mode pin. To force the buck converter into fixed frequency, PWM mode pull the MODE pin high.
5, 9	GND	Ground pin.
6	CE	Chip enable; Logic High enables step-down converter and LDO.
7	IN_BUCK	Input supply voltage for the step-down converter.
8	LX	Switching node. Connect the inductor to this pin. It is internally connected to the drain of both high- and low-side MOSFETs.

Pin Configuration

WLCSP-9
(Top View)



Absolute Maximum Ratings[1]

T_A = 25°C unless otherwise noted.

Symbol	Description	Value	Units
V_{IN_BUCK}, V_{IN_LDO}	Input Voltage	-0.3 to 6.0	V
V_{LX}	LX to GND	-0.3 to V_{IN} + 0.3	
V_{OUT_BUCK}	OUT_BUCK to GND	-0.3 to V_{IN} + 0.3	
V_{OUT_LDO}	OUT_LDO to GND	-0.3 to V_{IN} + 0.3	
V_{CE}, V_{MODE}	CE to GND	-0.3 to V_{IN} + 0.3	
T_J	Maximum Junction Operating temperature	-40 to +150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	300	

Thermal Information[3]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance[4]	284	°C/W
P_D	Maximum Power Dissipation	352	mW

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum Rating should be applied at any one time.
2. Based on long-term current density limitation.
3. Mounted on an FR4 board.
4. Derate 20mW/°C above 25°C.

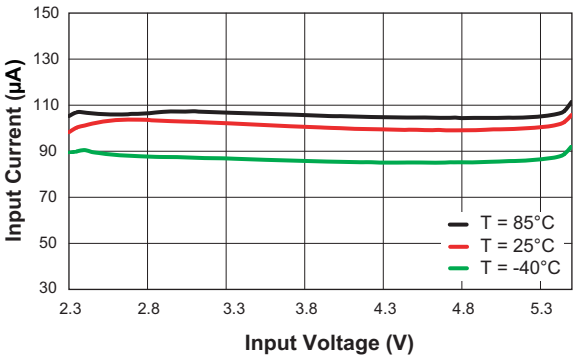
Electrical Characteristics[1]

V_{IN} = 3.6V; C_{IN} = C_{OUT_BUCK} = 4.7µF; C_{IN_LDO} = 1.0µF; C_{OUT_LDO} = 2.2µF; T_A = -40°C to 85°C unless otherwise noted. Typical values are at T_A = 25°C.

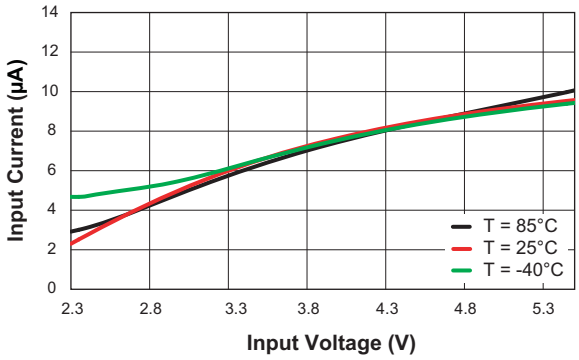
Symbol	Description	Conditions	Min	Typ	Max	Units
Step-Down Converter						
V_{IN_BUCK}	Input Voltage		2.3		5.5	V
$V_{OUT\_BUCK\_ACC}$	Output Voltage Accuracy	V_{IN} = 3.6V, 1mA Load, T_A = 25°C, PWM Mode	591	600	609	mV
$V_{OUT\_BUCK\_TOL}$	Output Voltage Tolerance	0mA to 600mA load, V_{IN} = 2.5V to 5.5V	-3.0		3.0	%
$\Delta V_{OUTB}/\Delta V_{IN}$	Line Regulation	V_{IN} = 2.5V to 5.5V		0.1		%/V
I_{LIM}	P-Channel Current Limit		1000			mA
$R_{DS(ON)H}$	High Side Switch On Resistance			360		mΩ
$R_{DS(ON)L}$	Low Side Switch On Resistance			200		mΩ
I_{OUT_BUCK}	Out_BUCK Leakage Current	V_{out_BUCK} = 1.8V			20	µA
T_S	Start-Up Time	From Enable to Output Regulation		50		µs
F_{OSC}	Oscillator Frequency	T_A = 25°C		3.0		MHz
LDO Regulator						
V_{IN_LDO}	Input Voltage		1.62		V_{IN_BUCK}	V
$V_{OUT\_LDO\_ACC}$	Output Voltage Accuracy	V_{IN_BUCK} = 3.6V, V_{IN_LDO} = 1.8V, 1mA Load, T_A = 25°C	-2		+2	%
$V_{OUT\_LDO\_TOL}$	Output Voltage Tolerance	0mA to 300mA load; V_{IN_LDO} = 2.5V to 5.5V	-3		+3	%
$\Delta V_{OUT}/\Delta V_{IN}$	Line Regulation	V_{INL} = 2.5V to 5.5V		0.6		%/V
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	0mA to 300mA load		1.2		%
$I_{OUT(MAX)}$	Maximum Output Current		300			mA
I_{LIM}	Output Current Limit			1		A
V_{DO}	Dropout Voltage	V_{IN_BUCK} = 3.6V, V_{IN_LDO} = 1.8V, 200mA load		300		mV
System Quiescent Curent						
I_Q	System Quiescent Current	V_{OUT_BUCK} = 1.8V, No load on LDO, LL Mode		100		µA
		PWM Mode		7		mA
I_{SHDN}	Shutdown Current	V_{CE} = GND			1	µA
Logic						
$V_{CE(L)}$	Enable Threshold Low				0.4	V
$V_{CE(H)}$	Enable Threshold High		1.4			V
I_{CE}	Input Low Current	V_{IN} = V_{OUT} = 5.5V	-1.0		1.0	µA
Thermal						
T_{SD}	Over-Temperature Shutdown Threshold			140		°C
T_{HYS}	Over-Temperature Shutdown Hysteresis			15		°C

Typical Characteristics

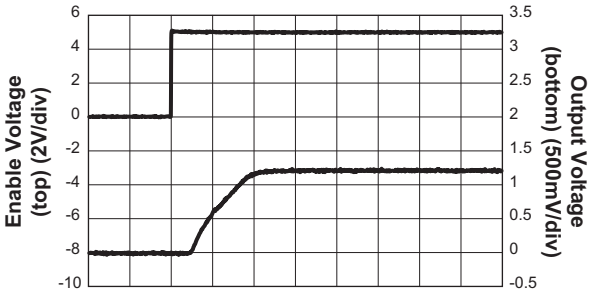
No Load Quiescent Current vs. Input Voltage
(EN_BUCK = EN_LDO = V_{IN}; LL Mode)



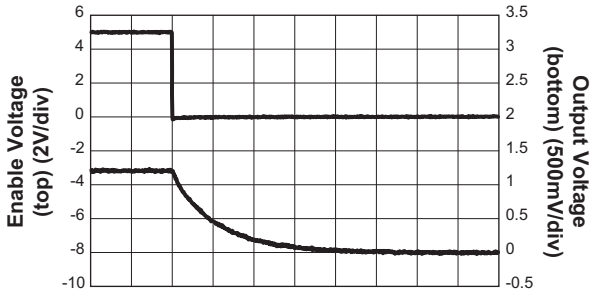
No Load Quiescent Current vs. Input Voltage
(EN_BUCK = EN_LDO = V_{IN}; PWM Mode)



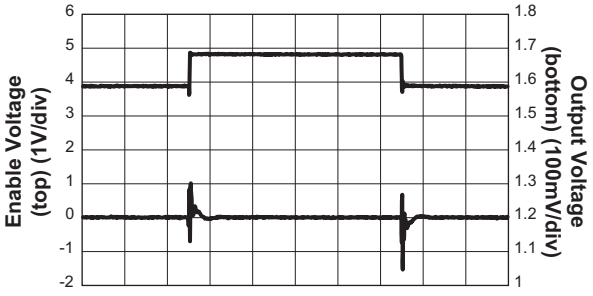
LDO Turn-On Response Time
(V_{OUT} = 1.2V; V_{IN} = 5V; I_{OUT} = 400mA)



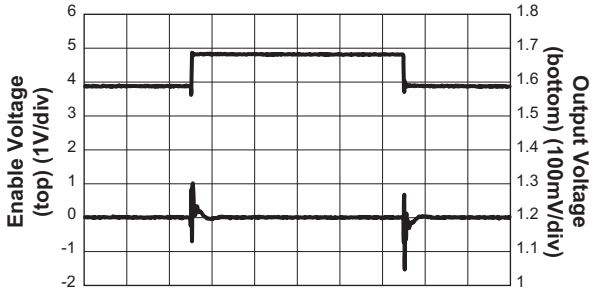
LDO Turn-Off Response Time
(V_{OUT} = 1.2V; V_{IN} = 5V; I_{OUT} = 400mA)



LDO Line Transient Response
(V_{OUT} = 1.2V; V_{IN} = 4V to 5V; I_{OUT} = 400mA)

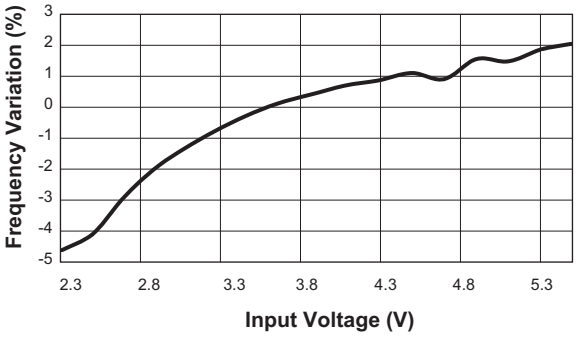


LDO Line Transient Response
(V_{OUT} = 1.2V; V_{IN} = 4V to 5V; I_{OUT} = 400mA)

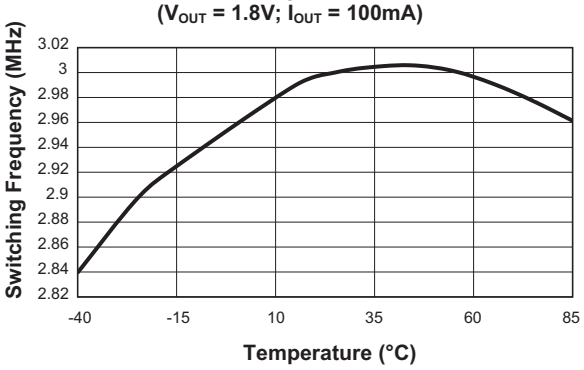


Typical Characteristics

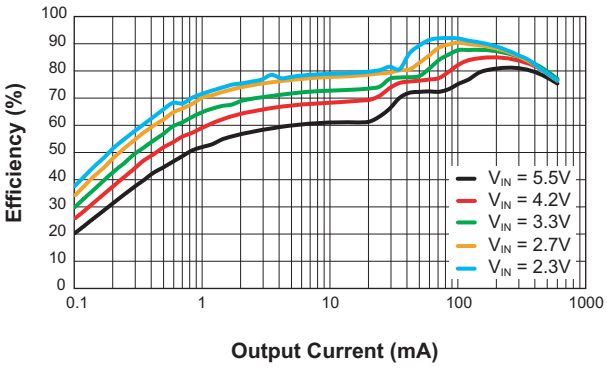
Step-Down Converter Switching Frequency vs. Input Voltage
(V_{OUT} = 1.8V; I_{OUT} = 100mA)



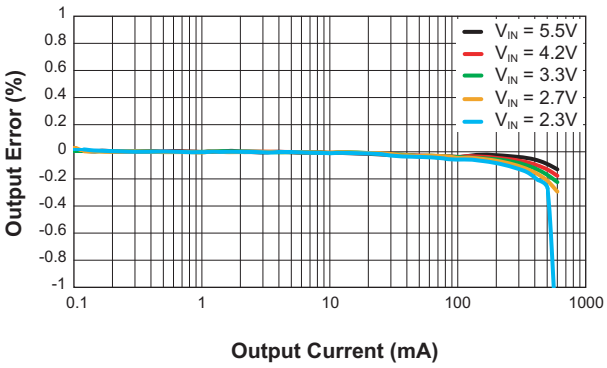
Step-Down Converter Switching Frequency vs. Temperature
(V_{OUT} = 1.8V; I_{OUT} = 100mA)



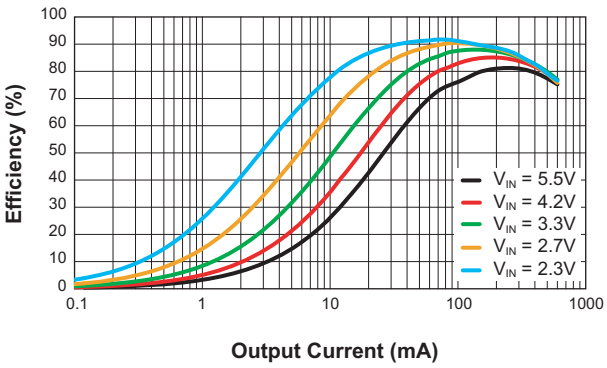
Step-Down Converter Efficiency vs. Load
(V_{OUT} = 1.8V; L = 2.2µH; LL Mode)



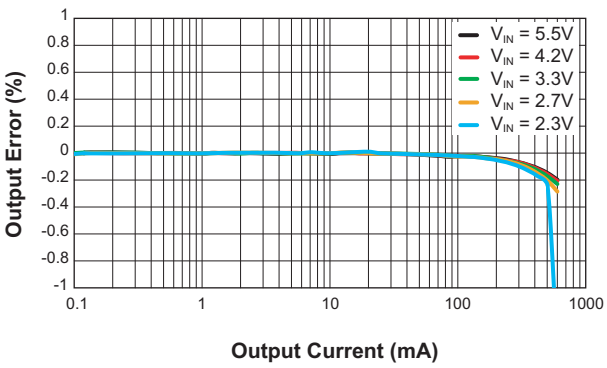
Step-Down Converter DC Regulation
(V_{OUT} = 1.8V; L = 2.2µH; LL Mode)



Step-Down Converter Efficiency vs. Load
(V_{OUT} = 1.8V; L = 2.2µH; PWM Mode)

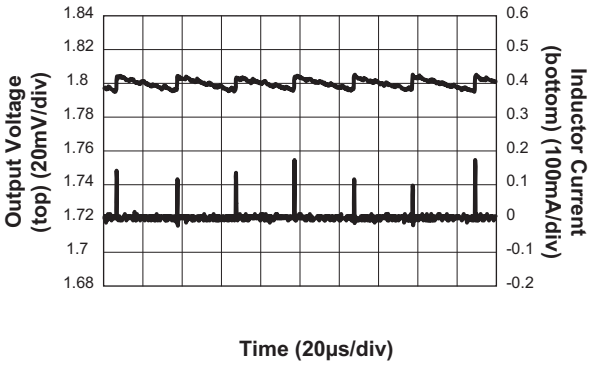


Step-Down Converter DC Regulation
(V_{OUT} = 1.8V; L = 2.2µH; PWM Mode)

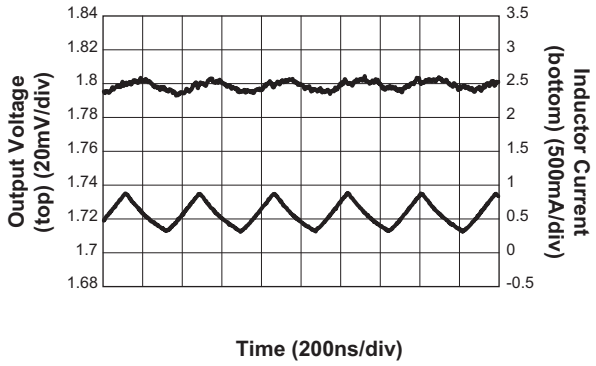


Typical Characteristics

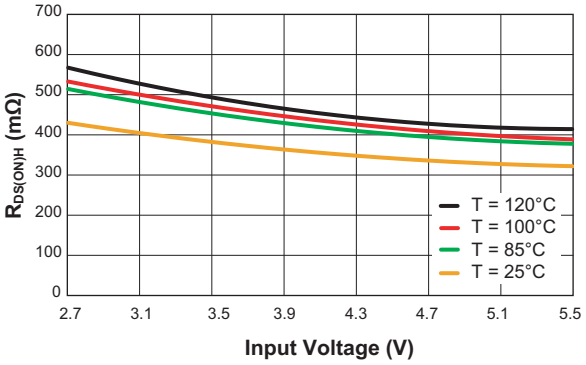
Step-Down Converter Output Ripple
(V_{OUT} = 1.8V; V_{IN} = 5V; I_{OUT} = 1mA)



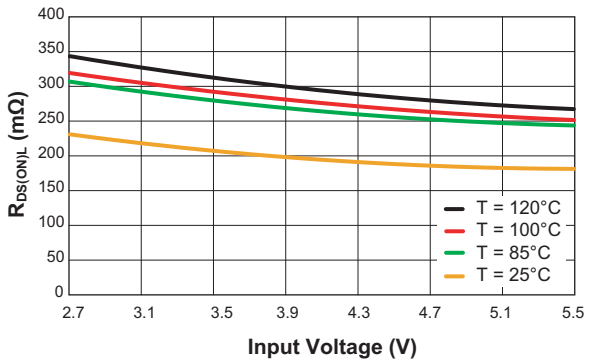
Step-Down Converter Output Ripple
(V_{OUT} = 1.8V; V_{IN} = 5V; I_{OUT} = 600mA)



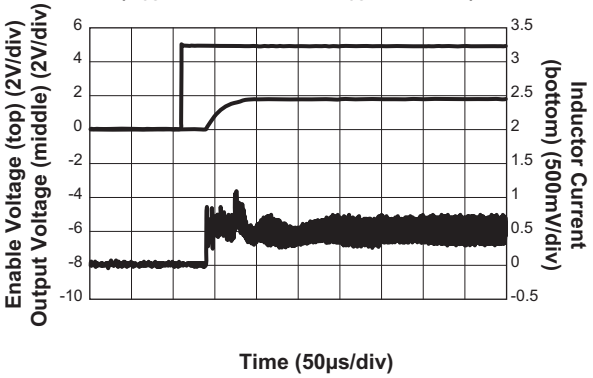
Step-Down Converter P-Channel $R_{DS(ON)}$ vs. Input Voltage



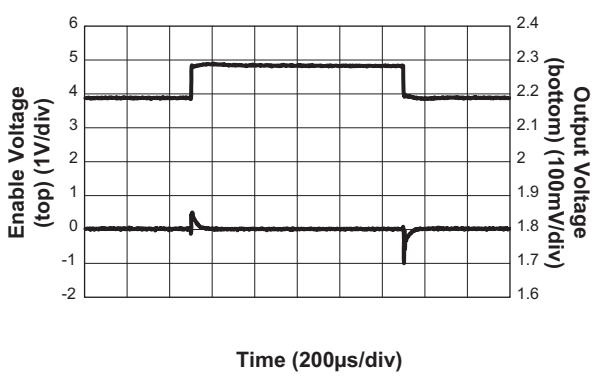
Step-Down Converter N-Channel $R_{DS(ON)}$ vs. Input Voltage



Step-Down Converter Soft Start
(V_{OUT} = 1.8V; V_{IN} = 5V; I_{OUT} = 600mA)

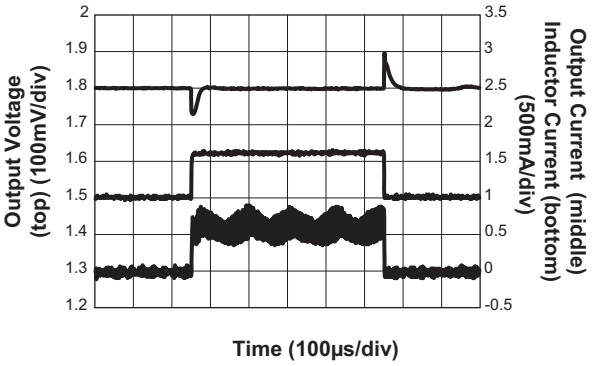


Step-Down Converter Line Transient Response
(V_{OUT} = 1.2V; V_{IN} = 4V to 5V; I_{OUT} = 600mA)

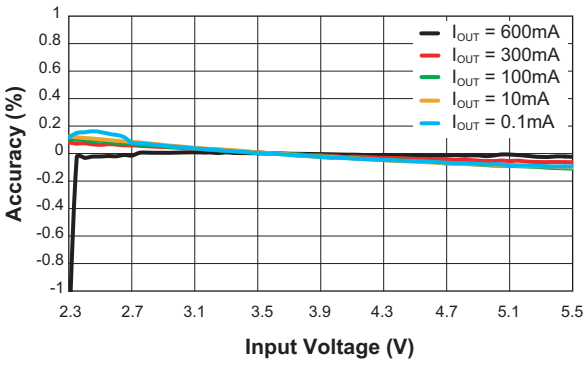


Typical Characteristics

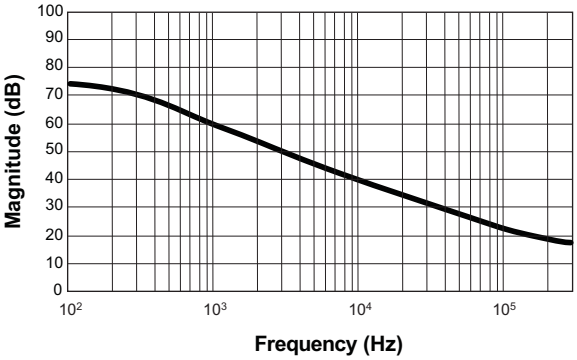
Step-Down Converter Load Transient Response
(V_{OUT} = 1.8V; V_{IN} = 5V; I_{OUT} = 1mA to 600mA; C_{FF} = 0pF)



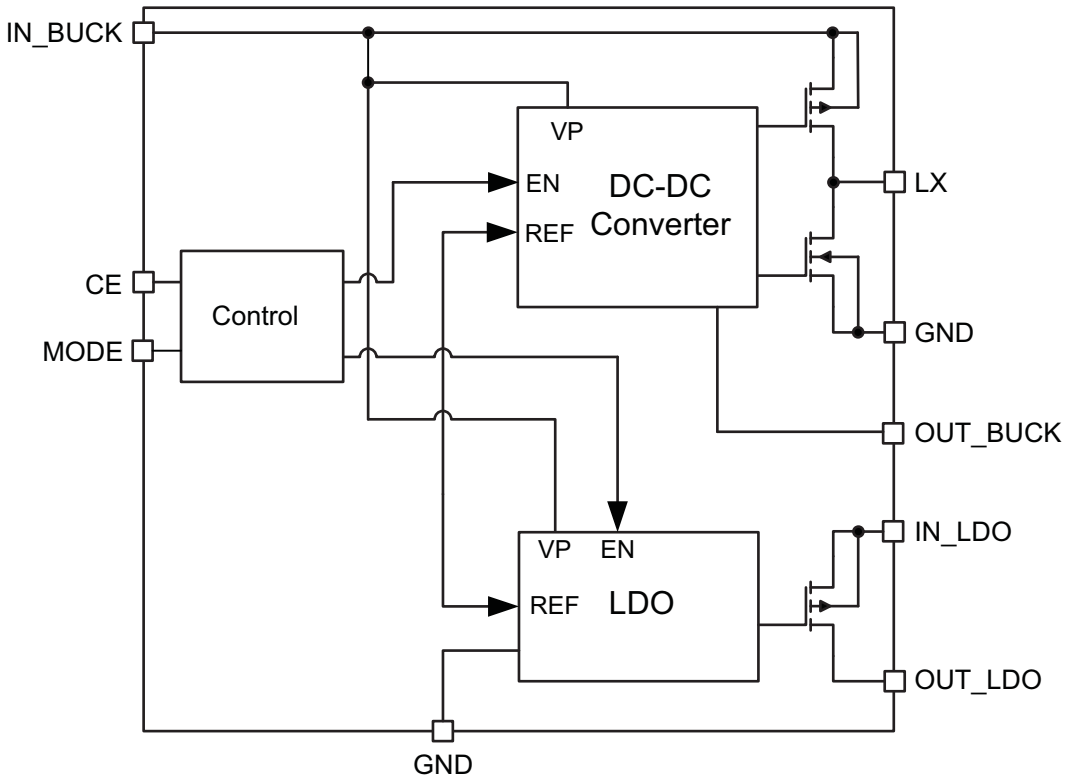
Step-Down Converter Line Regulation
(V_{OUT} = 1.8V; L = 2.2µH)



LDO Power Supply Rejection Ratio, PSRR
(I_{OUT2} = 1.8V; BW = 100Hz to 300Hz)



Functional Block Diagram



Functional Description

The AAT2749 is a two channel power converter that operates from a 2.3V to 5.5V power supply. The AAT2749 step-down converters can deliver up to 600mA while the LDO regulator can deliver up to 300mA. The typical no load quiescent current is 100µA for both the step-down converter and LDO regulator.

Step-Down Regulator

The AAT2749 contains a high performance 600mA, 3.0MHz monolithic step-down converter. Typically, a 2.2µH inductor and a 4.7µF ceramic capacitor are recommended (see table of values).

At dropout, the converter duty cycle increases to 100% and the output voltage tracks the input voltage minus the $R_{DS(ON)}$ drop of the P-channel high-side MOSFET. The input voltage range is 2.3V to 5.5V. The converter efficiency has been optimized for all load conditions, ranging from no load to 600mA.

The internal error amplifier and compensation provides excellent transient response, load, and line regulation. Soft start eliminates any output voltage overshoot when the enable or the input voltage is applied.

Mode Pin

To ensure high efficiency across the load range, the AAT2749 will automatically shift out of PWM mode in light load conditions. This mode of operation maintains high efficiency under light load conditions (typically <150mA). The MODE pin allows optional fixed frequency PWM mode for improved noise performance. This maintains constant frequency and low output ripple across all load conditions.

Control Loop

The AAT2749 step down converter is a peak current mode step-down converter. The current through the P-channel MOSFET (high side) is sensed for current loop control, as well as short circuit and overload protection.

The output of the voltage error amplifier programs the current mode loop for the necessary peak switch current to force a constant output voltage for all load and line conditions. Internal loop compensation terminates the trans-conductance voltage error amplifier output.

Soft Start / Enable

Soft start limits the current surge seen at the input and eliminates output voltage overshoot. When disabled, the AAT2749 is in a low-power, non-switching state. The total input current during shutdown is less than 1µA.

Current Limit

For overload conditions, the peak input current is limited. To minimize power dissipation and stresses under current limit and short-circuit conditions, switching is terminated after entering current limit for a series of pulses. Switching is terminated for seven consecutive clock cycles after a current limit has been sensed for a series of four consecutive clock cycles.

LDO Regulator

The AAT2749 includes a low-dropout (LDO) linear regulator. The LDO regulator operates from 1.62V to 5.5V; however, V_{IN_LDO} cannot exceed the input voltage to the step-down regulator (V_{IN_BUCK}). The linear regulator output voltage is set by internal resistive voltage dividers. The LDO regulator consumes about 50µA of quiescent current.

The 300mA LDO regulator is stable with a 2.2µF ceramic output capacitor. The LDO regulator has a current limit to protect against short circuit conditions.

Over-Temperature Protection

Thermal protection completely disables the converters when internal dissipation becomes excessive. The junction over-temperature threshold is 140°C with 15°C of hysteresis. Once an over-temperature or over-current fault conditions is removed, the output voltage automatically recovers.

Chip Enable Pin (CE)

Logic High at CE pin enables step-down converter and LDO.

Applications Information

Step-Down Converter Inductor Selection

The step-down converter uses peak current mode control with slope compensation to maintain stability for duty cycles greater than 50%. The output inductor value must be selected so the inductor current down slope meets the internal slope compensation requirements.

The internal slope compensation for the adjustable and low voltage fixed versions of channel 1 is 0.75A/µs. This equates to a slope compensation that is 75% of the inductor current down slope for a 1.8V output and 2.2µH inductor.

$$m = \frac{0.75 \cdot V_O}{L} = \frac{0.75 \cdot 1.8V}{1.8\mu H} = 0.75\frac{A}{\mu s}$$

$$L = \frac{0.75 \cdot V_O}{m} = \frac{0.75 \cdot 1.8V}{0.75\frac{A}{\mu s}} = 1.8\mu H$$

The inductor should be set equal to the output voltage numeric value in micro henries (µH). This guarantees that there is sufficient internal slope compensation. Manufacturer's specifications list both the inductor DC current rating, which is a thermal limitation, and the peak current rating, which is determined by the saturation characteristics. The inductor should not show any appreciable saturation under normal load conditions. Some inductors may meet the peak and average current ratings yet result in excessive losses due to a high DCR. Always consider the losses associated with the DCR and its effect on the total converter efficiency when selecting an inductor.

Step-Down Converter Input Capacitor

Select a 2.2µF to 4.7µF X7R or X5R ceramic capacitor for the input. To estimate the required input capacitor size, determine the acceptable input ripple level (V_{PP}) and solve for C_{IN}. The calculated value varies with input voltage and is a maximum when V_{IN} is double the output voltage.

$$C_{IN} = \frac{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot F_S}$$

$$\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right) = \frac{1}{4} \text{ for } V_{IN} = 2 \cdot V_O$$

$$C_{IN(MIN)} = \frac{1}{\left(\frac{V_{PP}}{I_O} - ESR\right) \cdot 4 \cdot F_S}$$

Always examine the ceramic capacitor DC voltage coefficient characteristics when selecting the proper value. For example, the capacitance of a 10µF, 6.3V, X5R ceramic capacitor with 5.0V DC applied is actually about 6µF.

The maximum input capacitor RMS current is:

$$I_{RMS} = I_O \cdot \sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The input capacitor RMS ripple current varies with the input and output voltage and will always be less than or equal to half of the total DC load current.

$$\sqrt{\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)} = \sqrt{D \cdot (1 - D)} = \sqrt{0.5^2} = \frac{1}{2}$$

For $V_{IN} = 2 \cdot V_O$

$$I_{RMS(MAX)} = \frac{I_O}{2}$$

The term $\frac{V_O}{V_{IN}} \cdot \left(1 - \frac{V_O}{V_{IN}}\right)$ appears in both the input voltage ripple and input capacitor RMS current equations and is a maximum when V_O is twice V_{IN}. This is why the input voltage ripple and the input capacitor RMS current ripple are a maximum at 50% duty cycle.

The input capacitor provides a low impedance loop for the edges of pulsed current drawn by the AAT2749. Low ESR/ESL X7R and X5R ceramic capacitors are ideal for this function. To minimize stray inductance, the capacitor should be placed as closely as possible to the IC. This keeps the high frequency content of the input current localized, minimizing EMI and input voltage ripple. The proper placement of the input capacitor (C1) can be seen in the evaluation board layout in the Layout section of this datasheet.

A laboratory test set-up typically consists of two long wires running from the bench power supply to the evaluation board input voltage pins. The inductance of these wires, along with the low-ESR ceramic input capacitor, can create a high Q network that may affect converter performance. This problem often becomes apparent in the form of excessive ringing in the output voltage during load transients. Errors in the loop phase and gain measurements can also result. Since the inductance of a short PCB trace feeding the input voltage is significantly lower than the power leads from the bench power supply, most applications do not exhibit this problem.

In applications where the input power source lead inductance cannot be reduced to a level that does not affect the converter performance, a high ESR tantalum or aluminum electrolytic should be placed in parallel with the low ESR/ESL bypass ceramic capacitor. This dampens the high Q network and stabilizes the system.

Step-Down Converter Output Capacitor

The output capacitor limits the output ripple and provides holdup during large load transitions. A 2.2µF to 4.7µF X5R or X7R ceramic capacitor typically provides sufficient bulk capacitance to stabilize the output during large load transitions and has the ESR and ESL characteristics necessary for low output ripple.

The output voltage droop due to a load transient is dominated by the capacitance of the ceramic output capacitor. During a step increase in load current, the ceramic output capacitor alone supplies the load current until the loop responds. Within two or three switching cycles, the loop responds and the inductor current increases to match the load current demand. The relationship of the output voltage droop during the three switching cycles to the output capacitance can be estimated by:

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S}$$

Once the average inductor current increases to the DC load level, the output voltage recovers. The above equation establishes a limit on the minimum value for the output capacitor with respect to load transients.

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_S \cdot V_{IN(MAX)}}$$

The internal voltage loop compensation also limits the minimum output capacitor value to 10µF. This is due to its effect on the loop crossover frequency (bandwidth), phase margin, and gain margin. Increased output capacitance will reduce the crossover frequency with greater phase margin.

The maximum output capacitor RMS ripple current is given by:

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT} \cdot (V_{IN(MAX)} - V_{OUT})}{L \cdot F_S \cdot V_{IN(MAX)}}$$

Dissipation due to the RMS current in the ceramic output capacitor ESR is typically minimal, resulting in less than a few degrees rise in hot-spot temperature.

LDO Input Capacitor

Typically, a 1µF or larger capacitor is recommended for C_{IN} in most applications. A C_{IN} capacitor is not required for basic LDO regulator operation. However, if the AAT2749 is physically located more than three centimeters from an input power source, a C_{IN} capacitor will be needed for stable operation.

C_{IN} should be located as close to the device V_{IN} pin as possible. C_{IN} values greater than 1µF will offer superior input line transient response and will assist in maximizing the highest possible power supply ripple rejection. Ceramic, tantalum, or aluminum electrolytic capacitors may be selected for C_{IN}. There is no specific capacitor ESR requirement for C_{IN}. However, for 300mA LDO regulator output operation, ceramic capacitors are recommended for C_{IN} due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources, such as batteries in portable devices.

LDO Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required between the VOUT and GND pins. The C_{OUT} capacitor connection to the LDO regulator ground pin should be as close as possible for maximum device performance. The AAT2749 LDO has been specifically designed to function with very low ESR ceramic capacitors. For best performance, ceramic capacitors are recommended.

Typical output capacitor values for maximum output current conditions range from 1µF to 10µF. Applications utilizing the exceptionally low output noise and optimum power supply ripple rejection characteristics of the channel 2 should use 2.2µF or greater for C_{OUT}. If desired, C_{OUT} may be increased without limit. In low output current applications where output load is less than 10mA, the minimum value for C_{OUT} can be as low as 0.47µF.

LDO Enable Function

The AAT2749 features an LDO regulator enable/disable function. This pin (EN) is active high and is compatible with CMOS logic. To assure the LDO regulator will switch on, the EN turn-on control level must be greater than 1.5V. The LDO regulator will go into the disable shutdown mode when the voltage on the EN pin falls below 0.6V. If the enable function is not needed in a specific application, it may be tied to V_{IN} to keep the LDO regulator in a continuously on state. When the LDO regulator is in shutdown mode, an internal 1.5kΩ resistor is connected between VOUT and GND. This is intended to discharge C_{OUT} when the LDO regulator is disabled. The internal 1.5kΩ has no adverse effect on device turn-on time.

LDO Short-Circuit Protection

The AAT2749 LDO contains an internal short-circuit protection circuit that will trigger when the output load current exceeds the internal threshold limit. Under short-circuit conditions, the output of the LDO regulator will be current limited until the short-circuit condition is removed from the output or LDO regulator package power dissipation exceeds the device thermal limit.

LDO Thermal Protection

The AAT2749 LDO has an internal thermal protection circuit which will turn on when the device die temperature exceeds 150°C. The internal thermal protection circuit will actively turn off the LDO regulator output pass device to prevent the possibility of over temperature damage. The LDO regulator output will remain in a shutdown state until the internal die temperature falls back below the 150°C trip point. The combination and interaction between the short circuit and thermal protection systems allows the LDO regulator to withstand indefinite short-circuit conditions without sustaining permanent damage.

Thermal Calculations

There are three types of losses associated with the AAT2749 step-down converter: switching losses, conduction losses, and quiescent current losses. Conduction losses are associated with the $R_{DS(ON)}$ characteristics of the power output switching devices. Switching losses are dominated by the gate charge of the power output switching devices. At full load, assuming continuous conduction mode (CCM), a simplified form of the synchro-

nous step-down converter and LDO losses is given by:

$$P_{TOTAL} = \frac{I_{OUT1}^2 \cdot (R_{DS()ON)H} \cdot V_{OUT1} + R_{DS(ON)L} \cdot [V_{IN1} - V_{OUT1}])}{V_{IN1}}$$

$$+ (t_{SW} \cdot F_S \cdot I_{OUT1} + I_{Q1}) \cdot V_{IN1} + (V_{IN2} - V_{OUT2}) \cdot I_{OUT2}$$

I_{Q1} is the step-down converter and LDO quiescent current respectively. The term t_{SW} is used to estimate the full load step-down converter switching losses.

Since $R_{DS(ON)}$, quiescent current, and switching losses all vary with input voltage, the total losses should be investigated over the complete input voltage range.

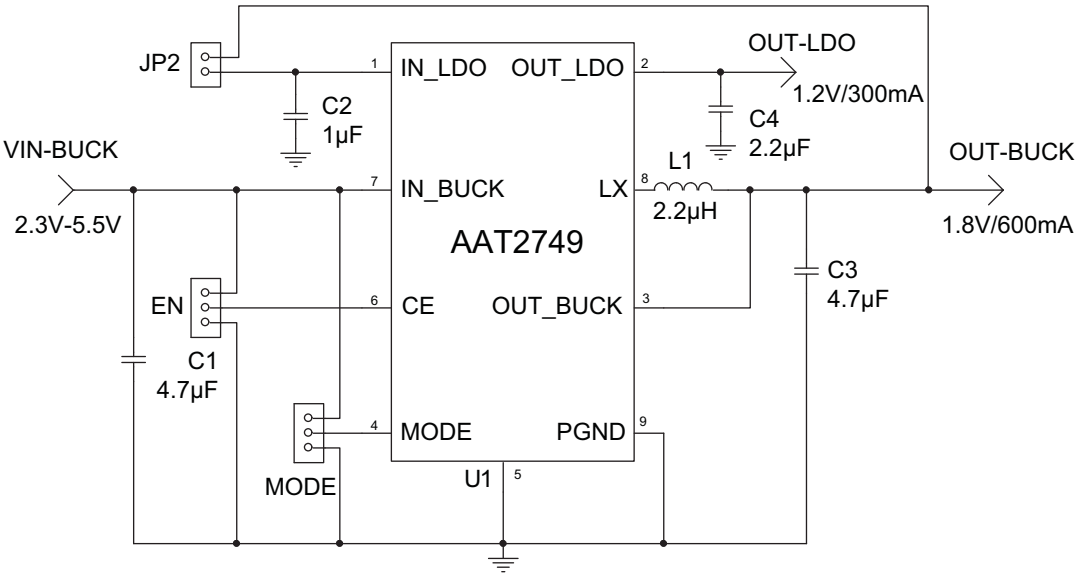
Given the total losses, the maximum junction temperature can be derived from the θ_{JA} for the CSP-9 package, which is 284°C/W.

$$T_{J(MAX)} = P_{TOTAL} \cdot \theta_{JA} + T_A$$

Layout Considerations

The suggested PCB layout for the AAT2749 is shown in Figures 2 and 3. The following guidelines should be used to help ensure a proper layout.

1. The bypass capacitors (C1, C2 and C4) should connect as closely as possible to input and output pin (Pins 1, 2, and 7) and PGND (Pin 9).
2. C3 and L1 should be connected as closely as possible. The connection of L1 to the LX pin should be as short as possible.
3. The feedback trace or OUT-BUCK pin (Pin 3) should be separated from any power trace and connected as closely as possible to the load point. Sensing along a high current load trace will degrade DC load regulation.
4. The resistance of the trace from the load return to PGND (Pin 9) should be kept to a minimum. This will help to minimize any error in DC regulation due to differences in the potential of the internal signal ground and the power ground.
5. The pad on the PCB for the CSP-9 package should use NSMD (non-solder mask defined) configuration due to its tighter control on the copper etch process. A pad thickness of less than 1 oz. is recommended to achieve higher stand-off. A high-density, small footprint layout can be achieved using an inexpensive, miniature, non-shielded, high DCR inductor.



U1	AAT2749 AnalogicTech, 300mA LDO and 600mA Buck Converter, CSP-9
C1, C3	Cap, MLC, 4.7µF/6.3V, 0805
C2	Cap, MLC, 1µF/6.3V, 0805
C3	Cap, MLC, 2.2µF/6.3V, 0805
L1	LQM2MPN2R2NGO, Murata, 2.2µH, I_{SAT} = 1.2A, DCR = 0.11Ω

Figure 2: AAT2749-IUR Evaluation Board Schematic and Bill of Materials (BOM).

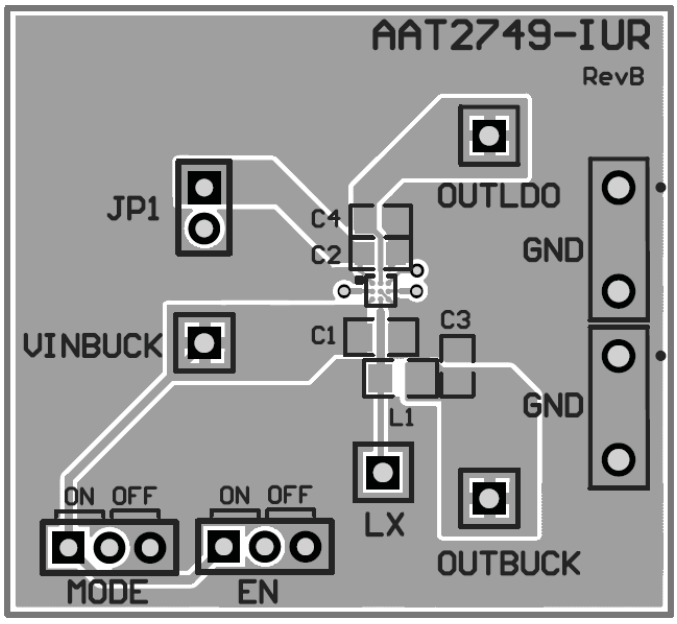


Figure 3: AAT2749-IUR Evaluation Board Top Layer.

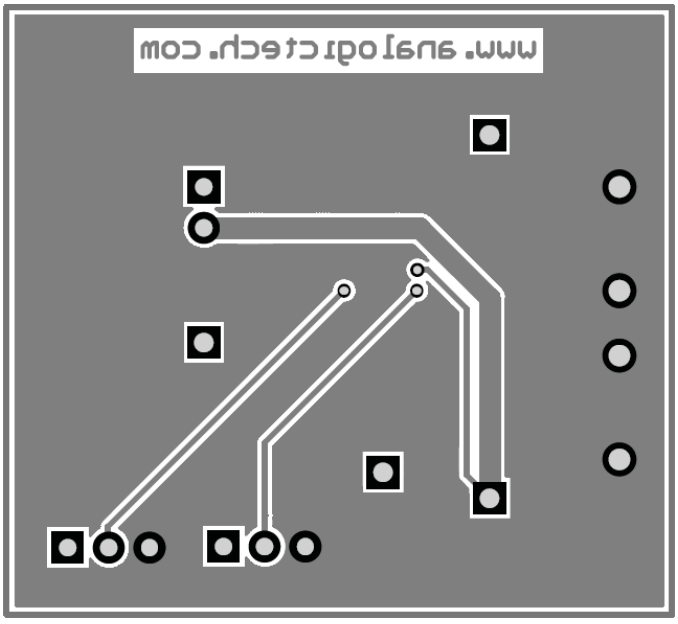


Figure 4: AAT2749-IUR Evaluation Board Bottom Layer.

AAT2749 Design Example

Specifications

V_{O1} = 1.8V @ 600mA, Pulsed Load ΔI_{LOAD} = 600mA
V_{O2} = 1.2V @ 300mA
V_{IN1} = 5V
F_S = 3MHz
T_{AMB} = 85°C in CSP-9 Package

Step-Down Converter Output Inductor

For Murata chip inductor LQM2MPN2R2NG0, 2.2µH, DCR = 0.11Ω.

$$\Delta I = \frac{V_{OUT1}}{L \cdot F_S} \cdot \left(1 - \frac{V_{OUT1}}{V_{IN1}}\right) = \frac{1.8V}{2.2\mu H \cdot 3MHz} \cdot \left(1 - \frac{1.8V}{5V}\right) = 174mA$$

$$I_{PK1} = I_{OUT1} + \frac{\Delta I}{2} = 600mA + 87mA = 687mA$$

$$P_{L1} = I_{OUT1}^2 \cdot DCR = 600mA^2 \cdot 111m\Omega = 40mW$$

Step-Down Converter Output Capacitor

V_{DROOP} = 0.18V (10% Output Voltage)

$$C_{OUT} = \frac{3 \cdot \Delta I_{LOAD}}{V_{DROOP} \cdot F_S} = \frac{3 \cdot 600mA}{0.18V \cdot 3MHz} = 3\mu F; \text{ use } 4.7\mu F$$

$$I_{RMS(MAX)} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{V_{OUT1} \cdot (V_{IN(MAX)} - V_{OUT1})}{L \cdot F_S \cdot V_{IN1(MAX)}} = \frac{1}{2 \cdot \sqrt{3}} \cdot \frac{1.8V \cdot (5.5V - 2.3V)}{2.2\mu H \cdot 3MHz \cdot 5.5V} = 46mA_{rms}$$

$$P_{RMS} = ESR \cdot I_{RMS}^2 = 5m\Omega \cdot (46mA)^2 = 11\mu W$$

Step-Down Converter Input Capacitor

Input Ripple V_{PP} = 10mV

$$C_{IN1} = \frac{1}{\left(\frac{V_{PP}}{I_{OUT1}} - ESR\right) \cdot 4 \cdot F_S} = \frac{1}{\left(\frac{10mV}{600mA} - 5m\Omega\right) \cdot 4 \cdot 3MHz} = 7\mu F; \text{ use } 4.7\mu F$$

$$I_{RMS} = \frac{I_{OUT1}}{2} = 300mA$$

$$P = ESR \cdot (I_{RMS}^2) = 5m\Omega \cdot (300mA)^2 = 0.31mW$$

AAT2749 Losses

All values assume 25°C ambient temperature and thermal resistance of 284°C/W in the CSP-9 package.

$$P_{TOTAL} = \frac{I_{OUT1}^2 \cdot (R_{DS(ON)H} \cdot V_{OUT1} + R_{DS(ON)L} \cdot [V_{IN1} - V_{OUT1}])}{V_{IN1}}$$

$$+ (t_{SW} \cdot F_S \cdot I_{OUT1} + I_{Q1}) \cdot V_{IN} + (V_{IN2} - V_{OUT2}) \cdot I_{OUT2}$$

$$= \frac{600mA^2 \cdot (360m\Omega \cdot 1.8V + 200m\Omega \cdot [5V - 1.8V])}{5V}$$

$$+ (5ns \cdot 3MHz \cdot 600mA + 100\mu A) \cdot 5V + (1.8V - 1.2V) \cdot 300mA$$

$$P_{TOTAL} = 318mW$$

$$T_{J(MAX)} = T_{AMB} + \Theta_{JA} \cdot P_{LOSS} = 25°C + (284°C/W) \cdot 318mW = 115°C$$

Ordering Information

Output Voltages		Package	Part Marking	Part Number (Tape and Reel)
V_{OUT_BUCK}	V_{OUT_LDO}			
1.8V	1.2V	WLCSP-9	6QXY	**AAT2749IUR-IE-T1**
1.8V	1.0V	WLCSP-9	7UXY	**AAT2749IUR-ID-T1**

Pb-free

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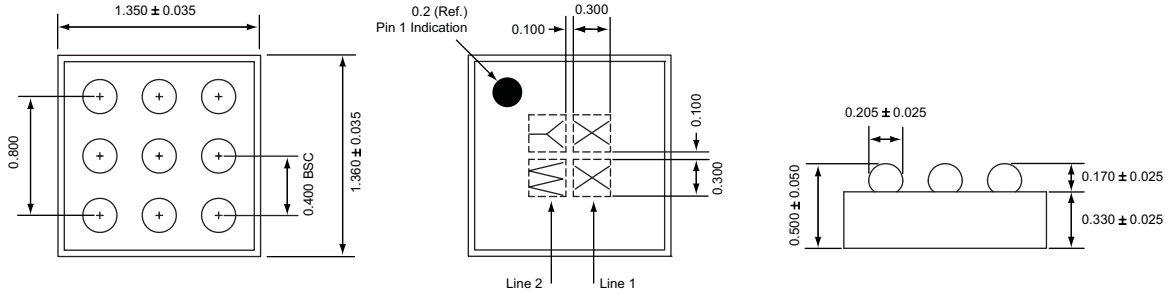
Package Information

WLCSP-9



Top View | Bottom View | Side View

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